Hi folks,

I have created a mute facility for the DF9NP PLL that will be activated with the absence or an impure 10 MHz signal attached to the board.

The solution is Simple.
The on board 5V supply to the buffer will be switched.
A track on the PCB with 5V needs to be cut and will be the spot where the FET must be installed, see attached Jpeg.
This will switch off the 5 Volt to the buffer etc.
So with no 5 Volt present it will effectively "switch off" the output of the PLL.
I have measured it and after careful investigations to monitor spurs coming out of the 49,152 MHz output. I am pleased to say, none were detected.

This circuit is necessary when you would like to operate the 9700 without a 10 MHz reference and with the DF9NP PLL board installed.
In a "no lock" situation the PLL loses control and generates a lot of noise and spikes. This ruins the performance of the IC9700 and creates a very dirty signal.

This simple solution on the board prevents such a situation from occurring.

1,7 Volt occurs in a PLL lock on the red LED to release the mute. This 1,7 Volt may not be loaded. This was one of the first challenges.
A simple transistor or Darlington will draw base current. This is not available.
Most MOSFET's have very high impedance on the gate, but need higher voltages on the gate to open the FET. The FET's I found could not drain the 60 mA current for the output circuit. So it had to be a dual stage solution.
The solution was the use of an opamp with a JFET input.
I had TL082 in the junkbox, but any other JFET opamp will do.
A TL082 is a dual opamp, you only need one half.

This opamp is configured as a comparator.
With around 1,2 Volt on the inverted input this works just fine.
A diode on the non-inverted input is needed. The voltage on the LED is not really 0 Volt in a no lock state. To prevent the opamp from switching on in a no lock situation the diode did a great job. Any Silicium diode will do. Most Silicium diodes need at least 0,6 Volt to conduct. Don't use germanium or shottkey diodes. They will conduct at much lower voltages. A 1N4148 will suffice.

The output of the opamp drives the gate of an IRFD110 FET. This FET has a low Vds on resistance. The output provides a little less than 4,75 Volts.
The loss in gain of the output stage from the PLL is less than 0,3 dB.

When a no lock state occurs on the PLL, the red LED is off. So the opamp has no output and the 5 Volt is off.
When the lock is established the opamp will open the FET and the 49,152 MHz output is generated. The LED on the source of the FET is optional and not really required. I used it while testing the circuit to see if the 5V switches on or off.
I managed to install all components on the board itself.
With some creativity this can achieved.

During my experiments I noticed that the reference input of the ADF4153 tried to lock on noise and/or anything else it detected.
This generated some output intermittently.
The input is a high impedance point with no termination.
I mounted a chip resistor of 50 Ohm between the two pins were the coax for the 10 MHz is attached. After this the ADF was much more stable and did not try to lock on spurious signals anymore. There was no difference in sensitivity on the 10 MHz input.

If you have any questions please do not hesitate to contact me

73, Peter PA2V